

# The ART of Power, Key to SoC Success

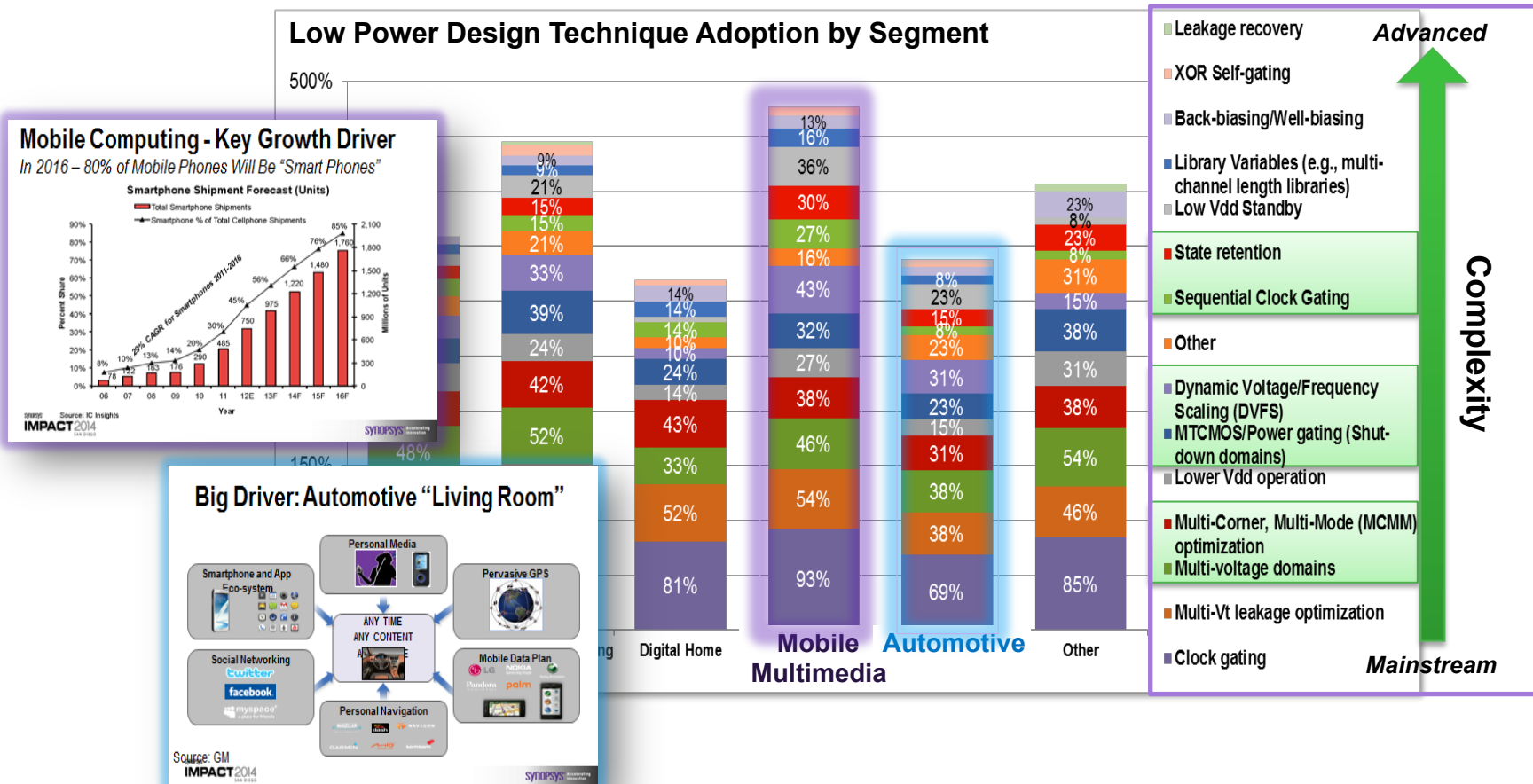
## Introduction to Low Power Verification Methodology

Rich Chang

Product Marketing, Verification Group

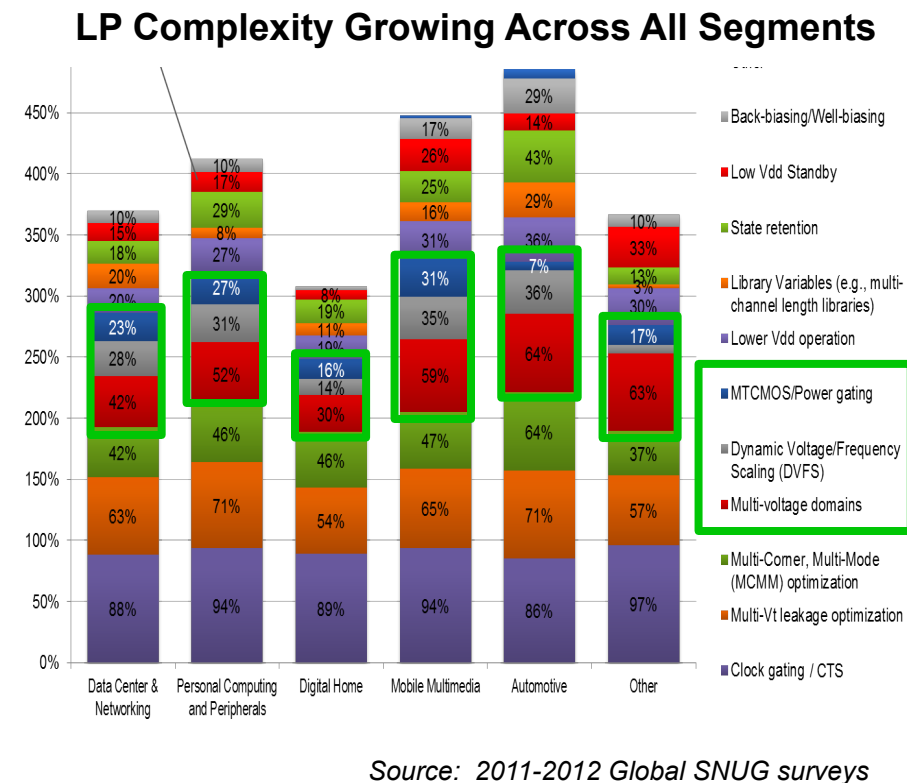
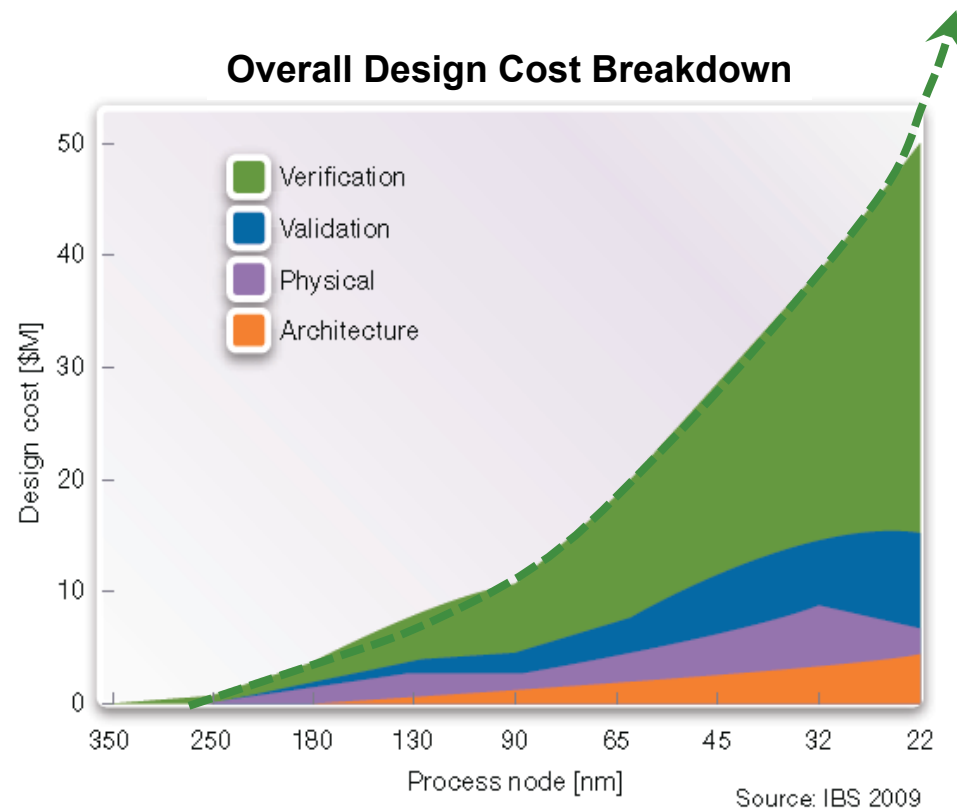


# Low Power is Everywhere



Mobile SoCs Driving Low Power Complexity Growth

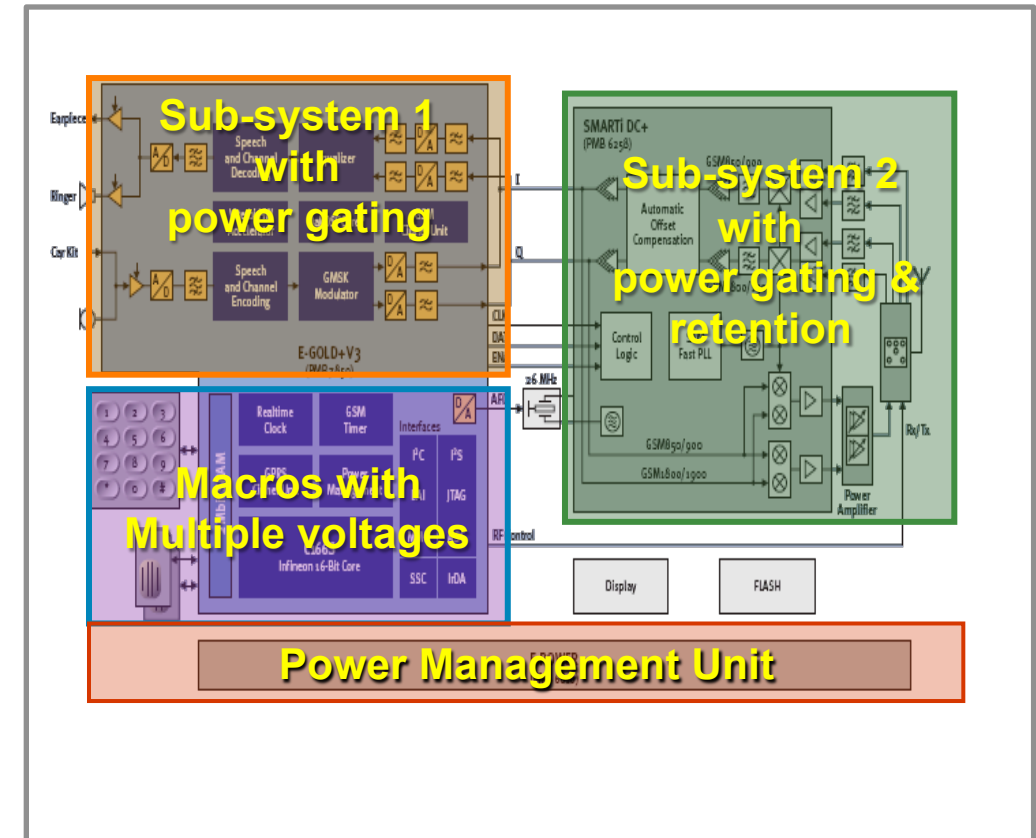
# Low Power Growth Driving Design Cost



Low power adoption causes increases in verification complexity

# Low Power Verification Requirements

- Power intent validation
  - Requires static verification
  - Debug and simulation of LP states (shutdown, standby, retention..) and low power cells
- Coverage of new low power states at sub system level and SoC level
- Protocol checks for transitions in / out of low power states



# Functional Intent vs. Power Intent

*What is the difference?*

## Functional Intent

- **Architecture**
  - Design hierarchy
  - Data path
  - Custom blocks
- **Application**
  - State machines
  - Combinatorial logic
  - I/Os
  - EX: CPU, DSP, Cache
- **Usage of IP**
  - Industry-standard interfaces
  - Memories
  - etc

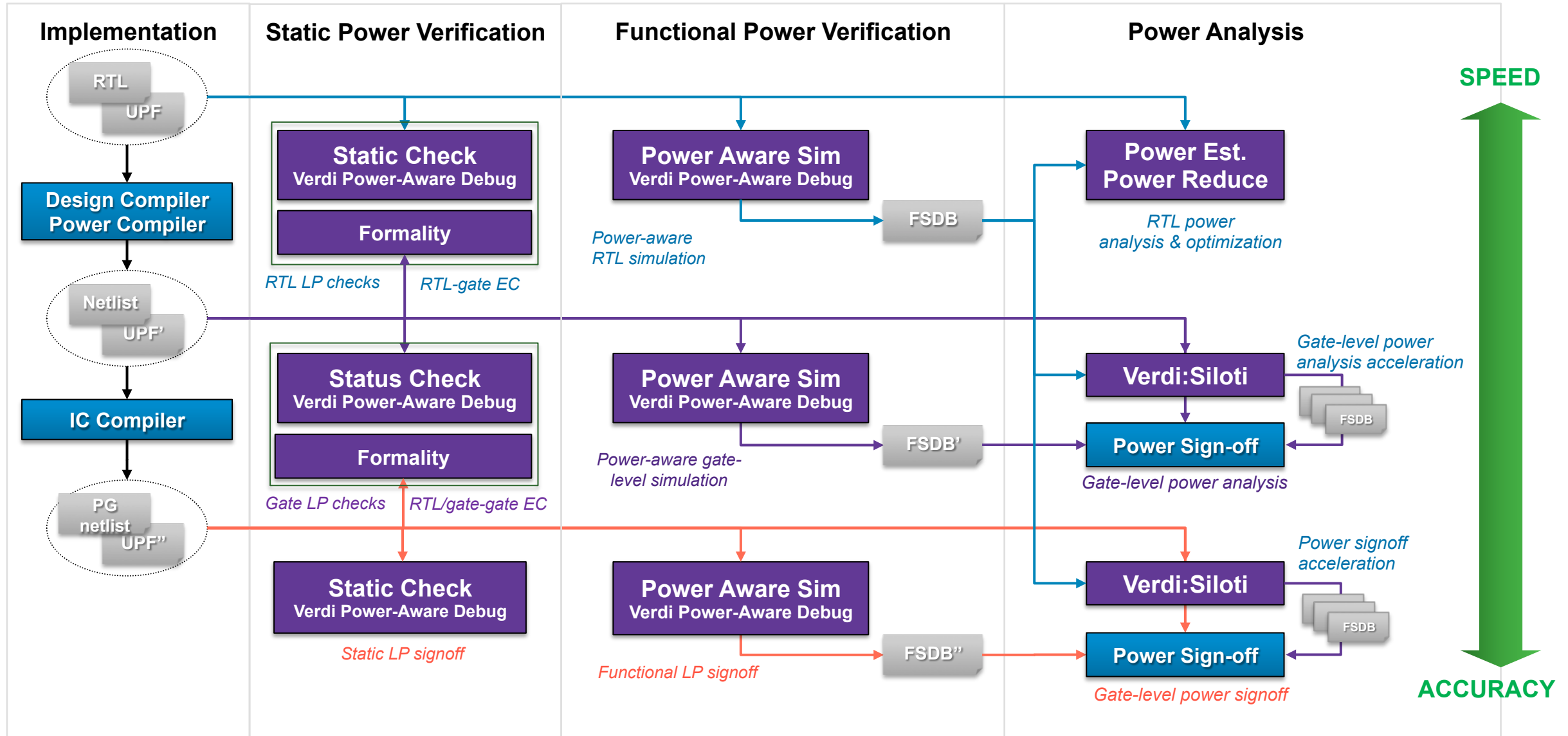
Captured in RTL

## Power Intent

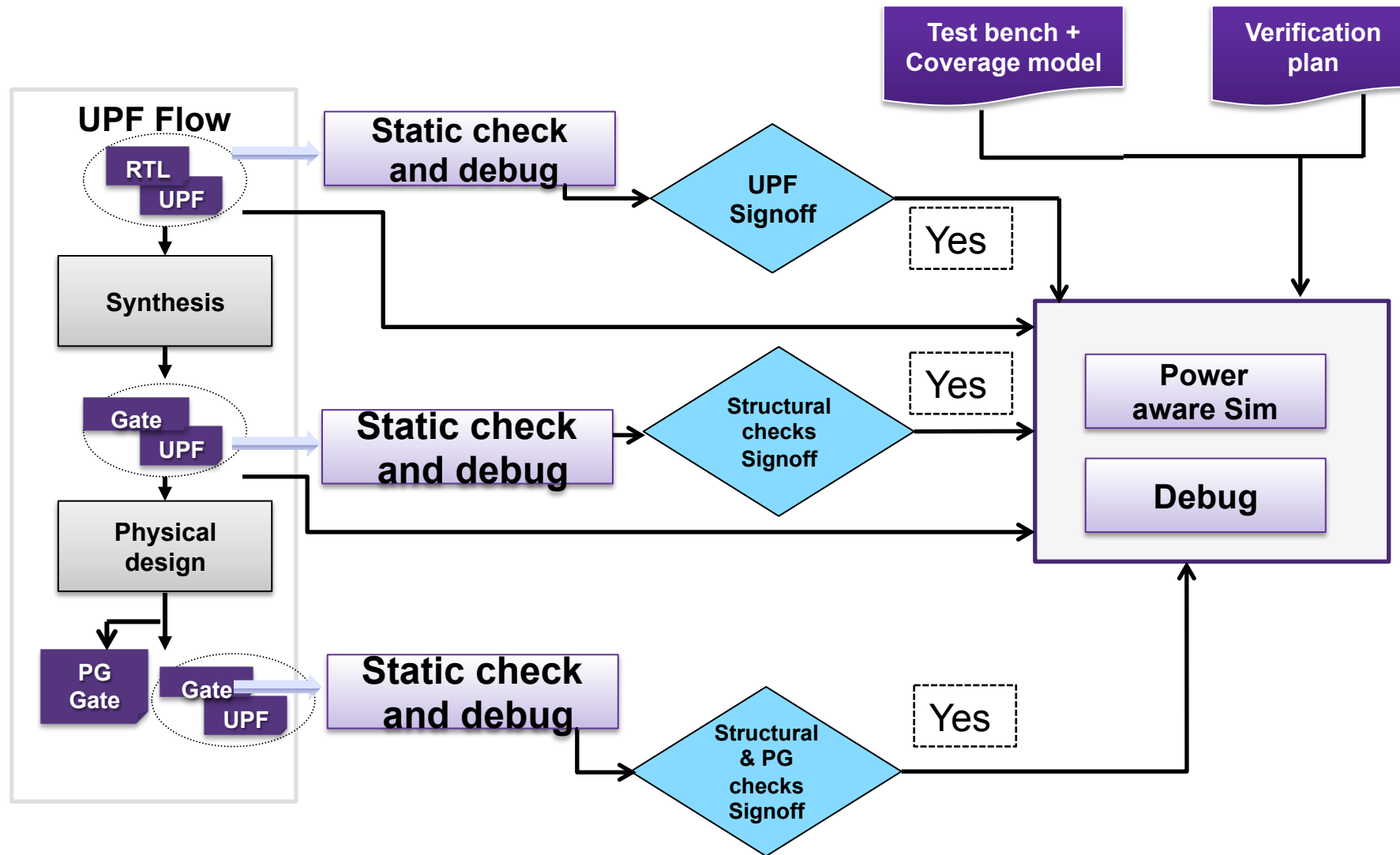
- **Power distribution architecture**
  - Power domains
  - Supply rails
  - Shutdown control
- **Power strategy**
  - Power state tables
  - Operating voltages
- **Usage of special cells**
  - Isolation cells, Level shifters
  - Power switches
  - Retention registers

Captured in UPF

# Synopsys Power Verification & Analysis Solutions



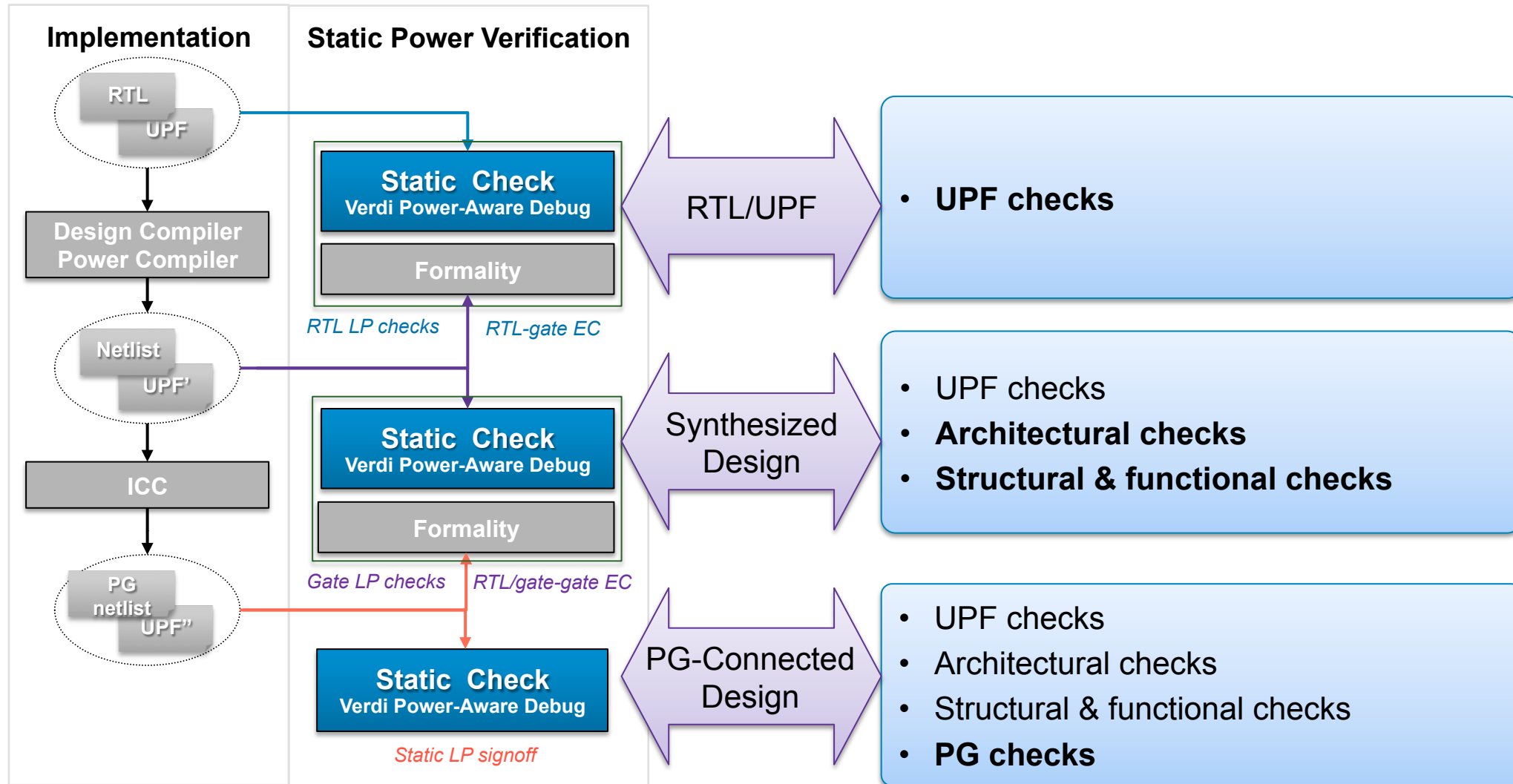
# Complete and Efficient Static and Dynamic Verification



# Static Power Verification



# Synopsys Static Low Power Verification



Continually verify consistency between design intent and implementation

# Static UPF Check

*Next-Generation Low Power Static Checking and Signoff*

## **Built from the ground-up for advanced SoCs**

- Capacity and performance for full-chip verification
- Next-gen data model and engines

## **Consistency and correlation with implementation**

- Design Compiler-like setup and use model
- Common format support: .lib, UPF, SDC, etc.
- Highly correlated hardware inference

## **Comprehensive set of applications**

- Low Power, Formal+Apps, CDC, Rule Checking
- Unified UPF reading across applications

## **Efficient debug and root cause analysis**

- Innovative LP-optimized error reporting and debugging

**3-5X Performance and Capacity Advantage**

# Static UPF Check

## *Features & Benefits*

### **SoC-Scale Performance & Capacity**

Loads full-chip SoCs at RTL and PG netlist—fast and complete checking through the entire design flow

### **DC TCL Support**

Use DC setup for fast adoption; easily integrated into Synopsys implementation flows

### **Accurate Hardware Inference**

Highest correlation of results between verification and implementation – Checks the right thing!

### **Production-Proven UPF Support**

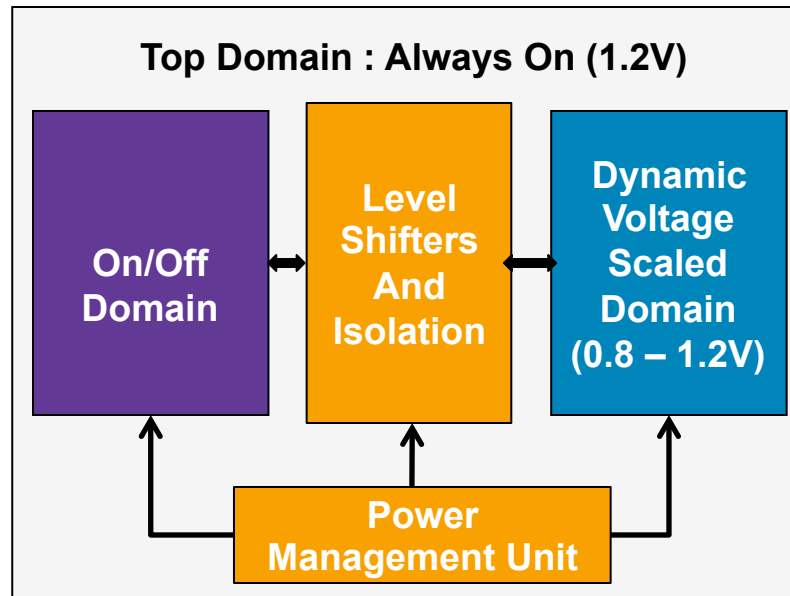
Best power network inference enables highest correlation to Synopsys low power implementation flows

### **Violation Noise Reduction Advanced LP Debug**

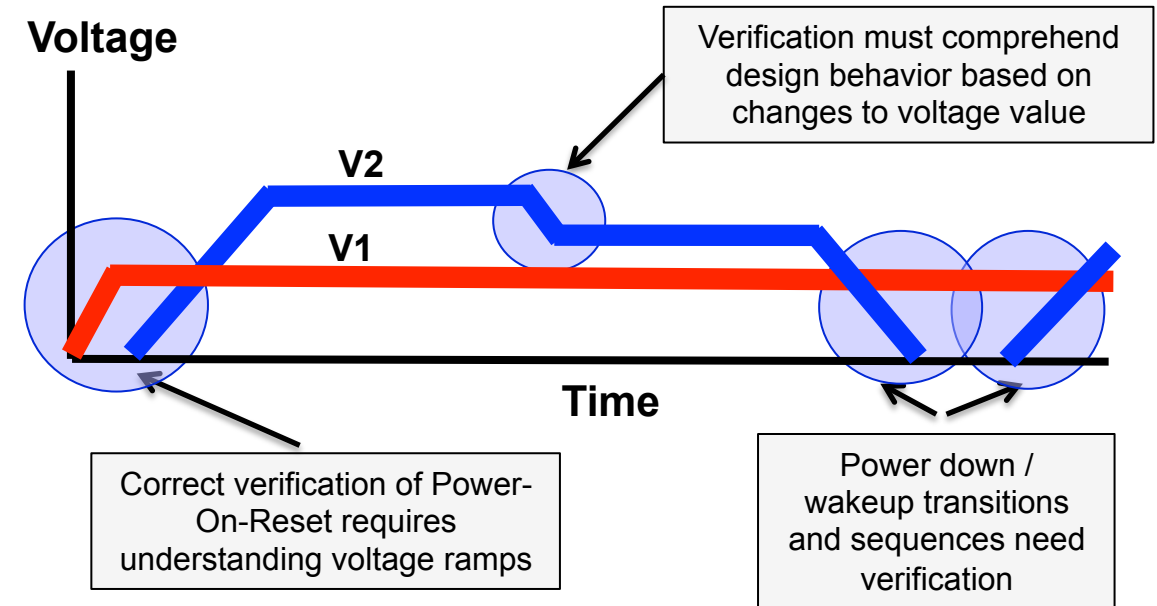
Easiest and fastest violation prioritization, debug and root cause analysis

# Dynamic Power Verification

# Accurate Power-Aware Simulation



Design



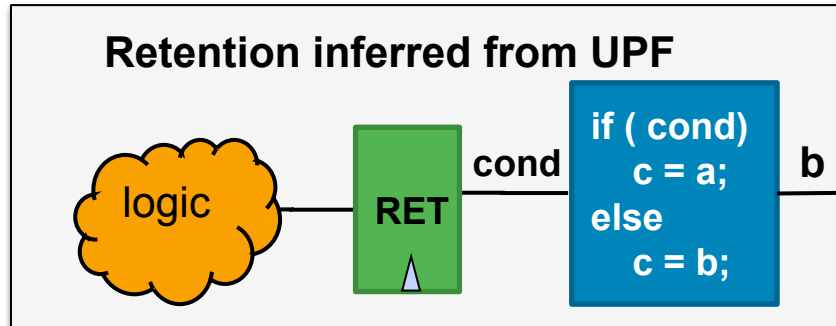
Verification

VCS NLP's true multi-voltage simulation verifies designs at all operating voltages / transitions

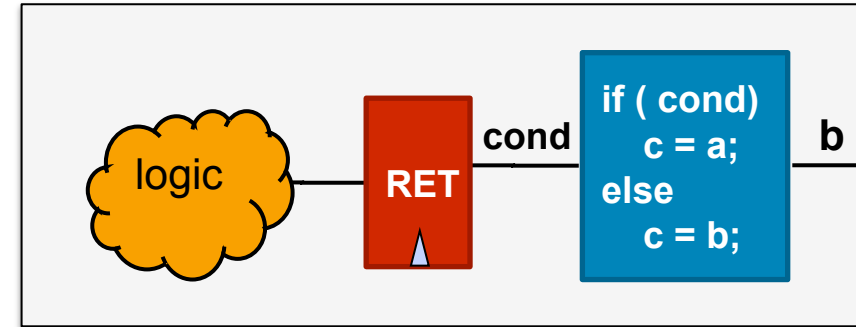
# Accurate Power Aware Simulation

*Native integration with advanced X-Prop catches X-optimism at RTL*

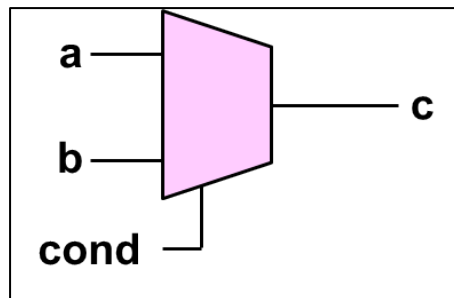
## Intended Design After Restore



## Actual Simulation After Restore



## Circuit 1



cond	a	b	c(RTL)	c(HW)	c(GLS with circuit 1)	c(with XPROP tmerge)
x	0	0	0	0	0	0
x	0	1	1	0/1	x	x
x	1	0	0	0/1	x	x
x	1	1	1	1	1	1

X-optimism at RTL caught !!

# Power Aware Simulation

## *Benefits*

### Highest Accuracy

Catch corner case LP bugs with voltage-aware simulation and comprehensive support for all advanced LP techniques

### High Performance

Enables broad use of LP simulation with the lowest impact on throughput and resources

### Unified UPF Support

Common UPF support enables unified LP verification with excellent ease-of-use and correlation across simulation and debug flows

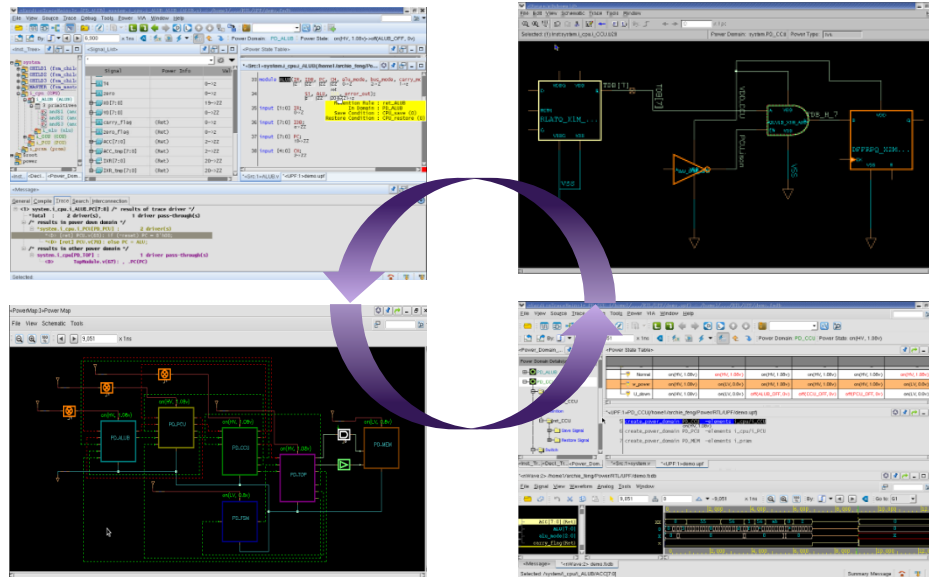
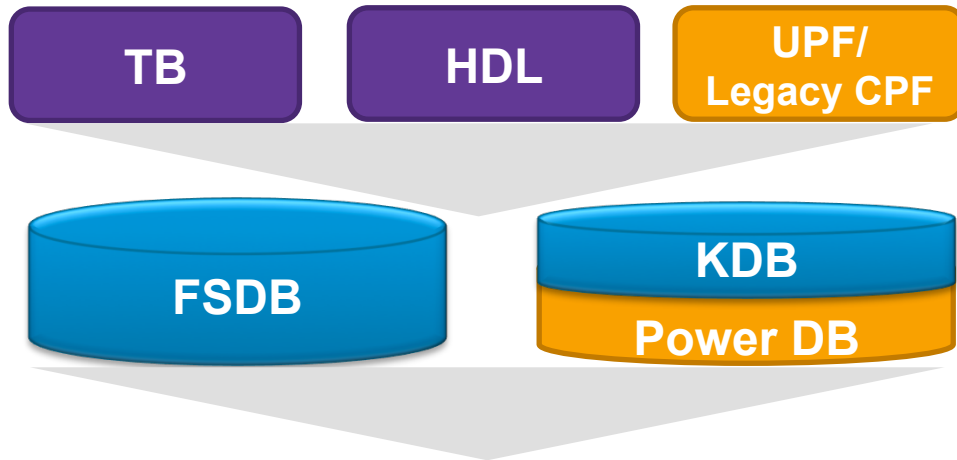
### LP Assertions and Coverage

Full LP planning and coverage features, and automated LP assertions enable comprehensive coverage-driven verification methodologies

### Advanced LP Debug

LP debug and coverage is natively integrated in Verdi, including power event visualization, powerful X-tracing, and cross-linking to UPF

# Power-Aware Debug



## Comprehensive Design Views

- Power-Aware Design Hierarchy
- Complete Schematic Views
- Annotated Power Intent

## Power Intent Visualization

- Power Manager Browser
- Power Map
- Impacted Signal Report

## Power-Aware Debug Automation

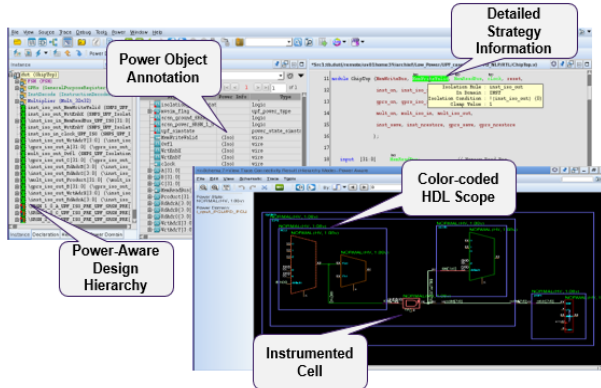
- Power-Aware Temporal Flow View
- Power Specific Waveform Debug
- Power Sequence Analysis



# Power-Aware Debug Highlights

## Comprehensive Design Views

Including Design and Instrumented Power Objects



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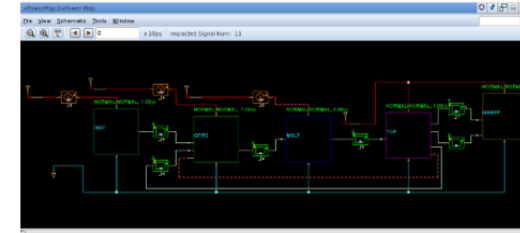
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- Unified design and power management hierarchy
- Integrated schematic views include power objects
  - Isolation cells
  - Retention cells
  - Level-Shifters etc.
- Annotations provide relevant power intent information

## Abstracted Power Domain View

Power Map



- Topology of design based on power domain including:
  - Connectivity of power domains
  - Isolation/Retention/Level-Shift/Repeater strategies
  - Power distribution network
  - Automatic highlighting of violations of isolation and level-shifter rules

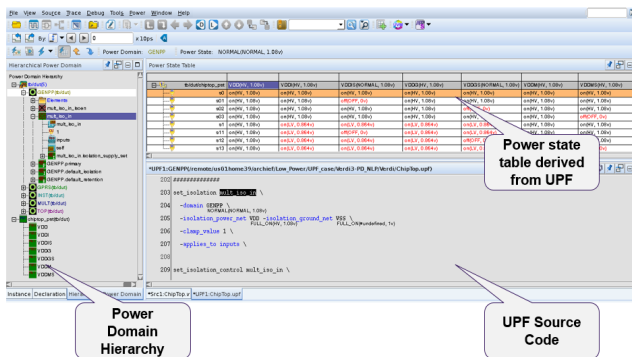
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## Dedicated Power Management Browser

Power Manager



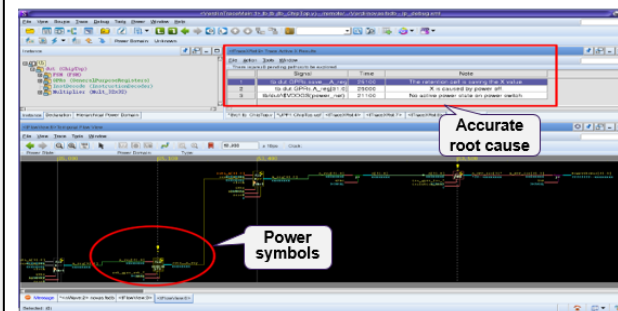
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- Power domain hierarchy including rules for
  - Isolation
  - Retention
  - Level-shift
  - Power switch
- UPF source code window for cross-reference
- Power state table derived from UPF for visualizing power mode transitions
  - Illegal state where mismatch occurred

## Power-Aware Temporal Flow View



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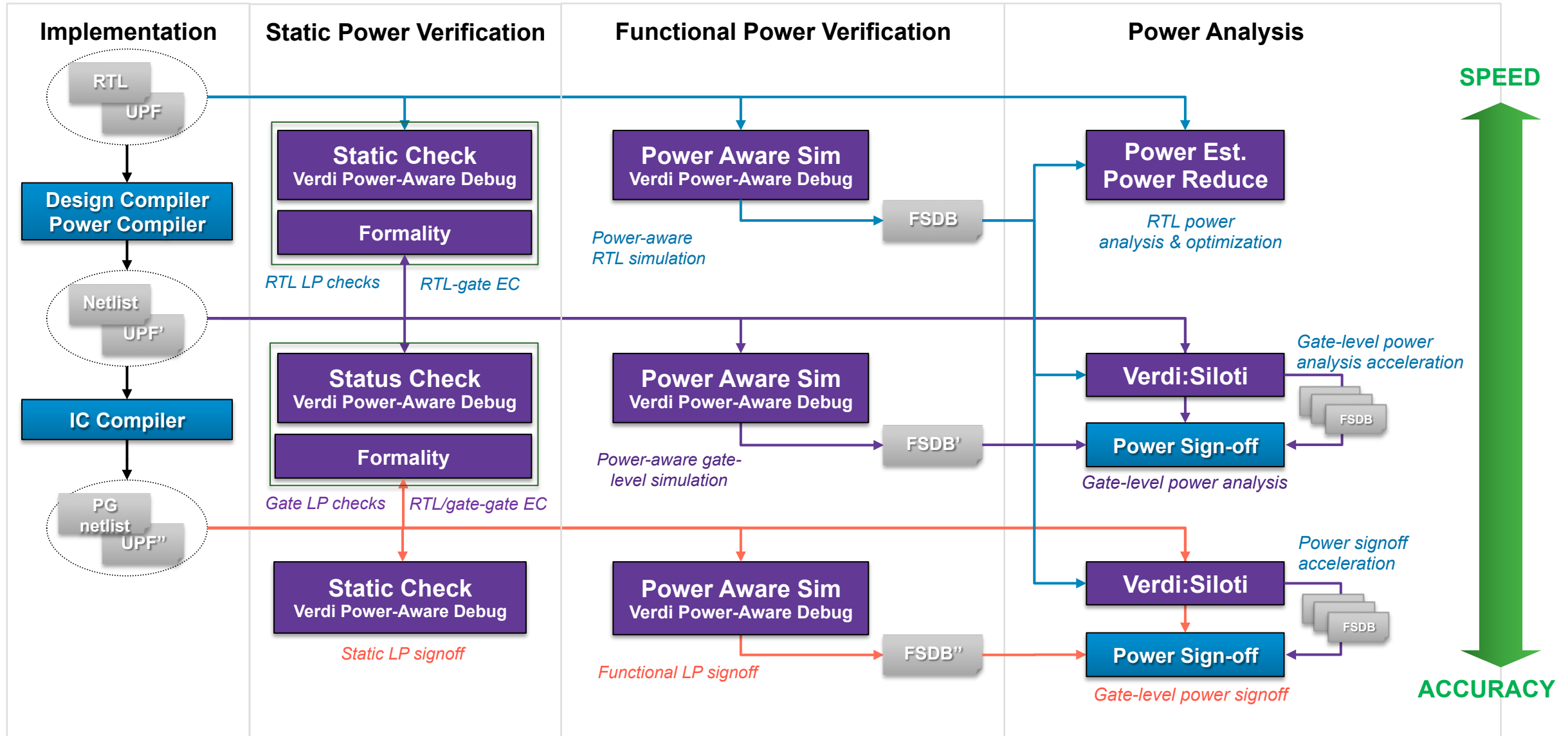
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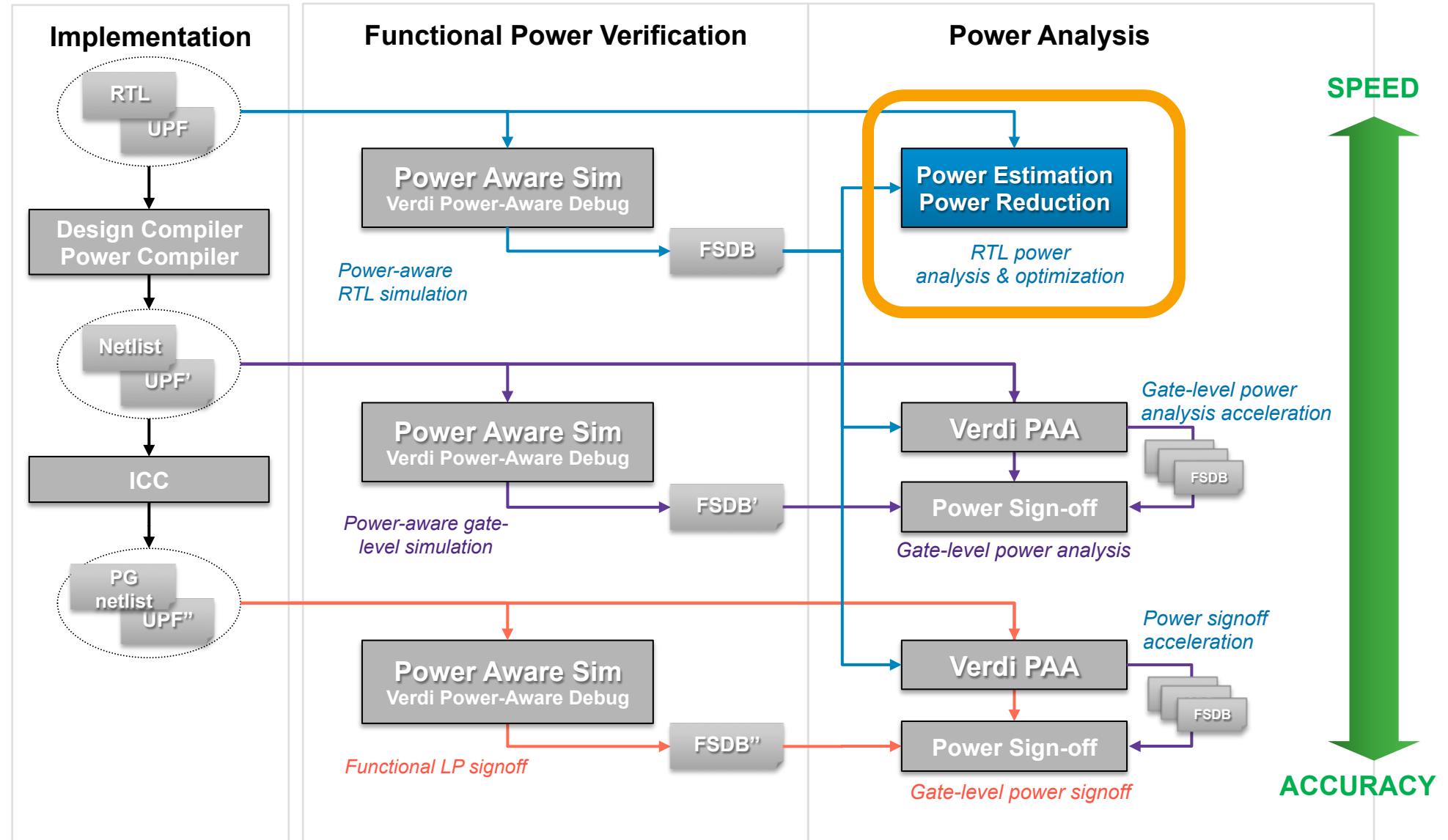
- Performs behavioral analysis on design, simulation AND power intent
- Automatically traces design behavior across multiple cycles
- Identifies root-cause taking instrumented cells and their values into consideration

# RTL Power Analysis & Optimization

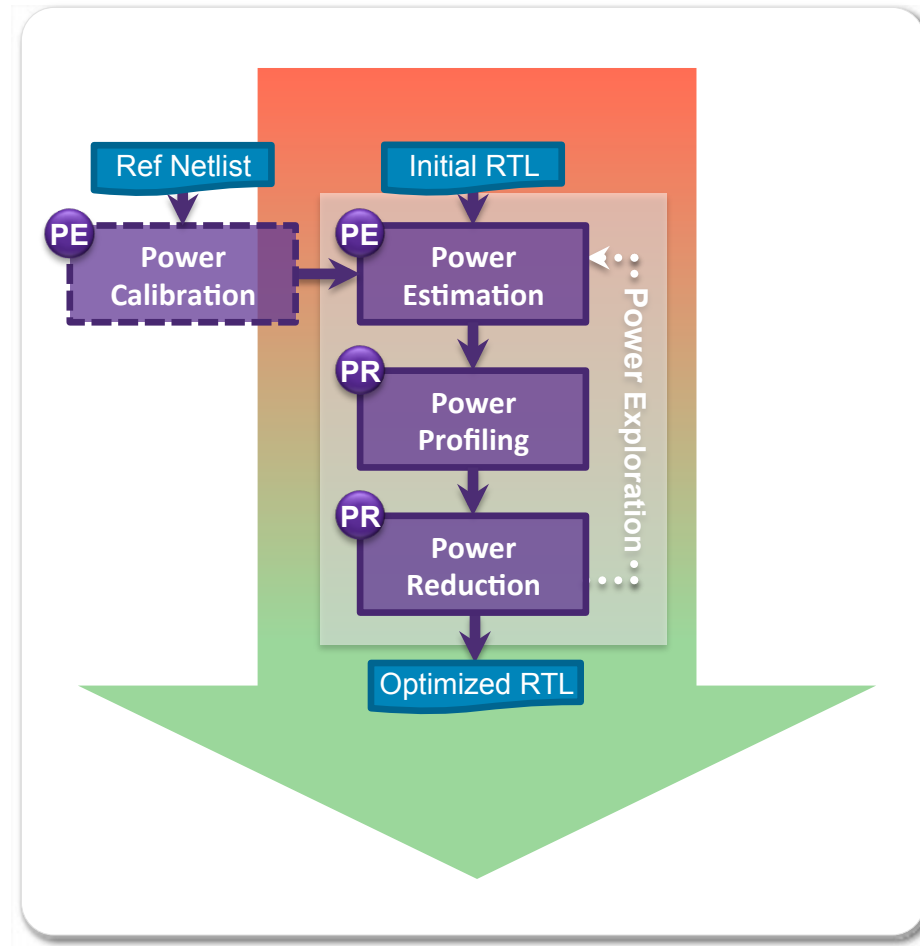
# Synopsys Power Verification & Analysis Solutions



# Synopsys Power Analysis Solutions

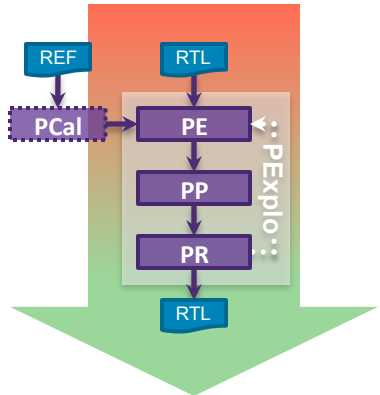


# RTL Power Optimization Flow



- PE SpyGlass Power Estimate
- PR SpyGlass Power Reduce
- Optional

# Designer View



SpyGlass Explorer: ethmac.prj <@engr1.sjc.atrenta.com>

File Edit View Tools Help Design Setup Goal Setup Analyze Results Reports

Run Goal: power/power\_est\_profiling@original Incremental Mode MS IS Waiver Design

sg\_shell> gui\_open\_power\_browser -rule PEPWR02 -tag AUTO\_LOAD\_BROWSER\_TAG -value auto\_load

sg\_shell> foreach\_in\_collection i [ get\_messages -of rule ... ] { if { [get\_attribute \$i msg] == "[Simulation file : /u/guillaume/TestCases/ethmac/spyglass/...]" } { [get\_attribute \$i msg] v1\_20150513\_1/demo\_designs/ethmac/spyglass/.../simulation ... Start time : 0.00ns, End time : 14603599.00ns } Average Leakage, Internal and Switching Power have been reported in the 'pe\_summary' report ( Leakage Power : '41.765uW' Internal Power : '738.312uW' Switching Power : '171.000uW' Total Power : ... )

Shell Waiver Tree Violations

Instances

ethmac

Instances

398 .Clk(wb\_clk\_i),  
399 .Reset(wb\_rst\_i),  
400 .Divider(r\_ClkDiv),  
401 .NoPre(r\_MiInoPre),  
402 .CtrlData(r\_CtrlData),  
403 .Rgnd(r\_RGAD),  
404 .FIad(r\_FIAD),  
405 .WCtrlData(r\_WCtrlData),

ethmac.v

Tcl Shell

Modular Schematic <@engr1.sjc.atrenta.com>

File Edit View Tools Help

SetRxClrq\_sync3\_reg

Clk

rtic\_N6885

SetRxClrq\_sync2

SDFFRX1

Sequential Block

Schematic

Update With Mouse Hover Selector...

Minimap

Power\_est Debug Data

Label	Value
Leakage Power	1.175e-06W
Internal Power	5.769e-07W
Switching Power	0.000e+00W
Total Power	5.887e-07W
Clock Gated	no
Clock Gating Efficiency	0.000



Power Explorer <@engr1.sjc.atrenta.com>

File View Help

Hierarchical Browser Clock Browser

Search in All columns Visualizations Configure Columns

Instance Hierarchy	Leakage	Total Dynamic	Number of Gat	Total Number	Percent Gated Re	Average Clock G	Average Register	Average Activity	Average
ethmac	41.765 uW	909.312 uW	1979	2604	75.998	73150	0.103	0.062	
local-logic	1.050 uW	31.989 uW	0	54	0.000	NA	0.017	0.244	
ethreg1	5.171 uW	48.112 uW	272	302	90.066	90.000	4.866e-05	6.637e-03	
maccontrol1	2.557 uW	12.981 uW	73	103	70.874	63.106	5.984e-07	1.314e-05	
macstatus1	602.712 nW	2.929 uW	6	18	33.333	33.333	0.000	1.100e-05	
mim1	3.890 uW	539.424 uW	178	334	53.298	49.379	0.779	0.539	
local-logic	3.075 uW	513.559 uW	148	294	50.340	47.787	0.879	0.718	
clkgen	282.848 nW	11.965 uW	0	9	0.000	NA	0.134	0.124	
outctrl	100.190 nW	5.133 uW	6	6	0.000	60.496	0.021	0.062	
shftreg	371.340 nW	8.766 uW	24	25	0.000	83.202	0.016	0.034	
rxethmac1	2.743 uW	25.328 uW	39	25	0.000	23.344	1.719e-05	2.374e-03	
bethmac1	3.148 uW	27.226 uW	39	25	0.000	25.266	0.016	4.888e-03	
wishbone	22.664 uW	221.324 uW	9	9	0.000	85.645	2.736e-03	5.166e-03	

Treemap

Treemap Area Criteria Total Area Treemap Color Criteria Average Clock Gating Efficiency(%)

Power Explorer



# Summary View

## SPYGLASS<sup>®</sup> FROM AURELIA Atrienta DashBoard - Spyglass Power Estimation/Reduction Report

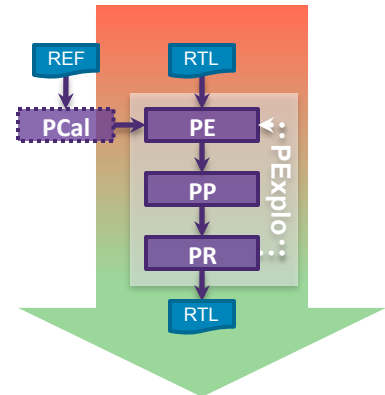
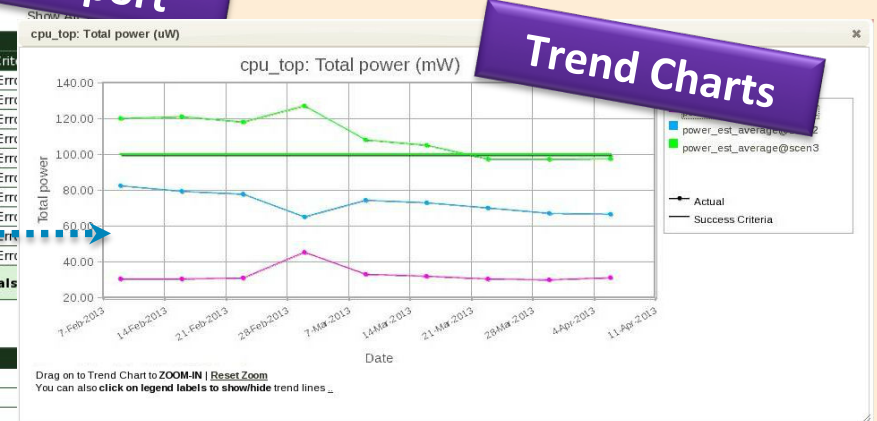
Pass / Fail Report

ethmac

Module: ethmac

Quality Goals	Run Completed At	Run Time	Run Status	Unresolved			Waived			Success Criteria
				fatal	error	warning	error	warning		
cdc_setup	N/A		Not started	0	0	0	0	0	0	Fatal=0, Err
power_est_average@original	05-20-2014 16:39:44	0:0:49 (49 secs)	Completed	0	0	9	0	0	0	Fatal=0, Err
cdc_verify_struct@original	N/A		Not started	0	0	0	0	0	0	Fatal=0, Err
power_profiling@original	05-20-2014 16:40:22	0:0:29 (29 secs)	Completed	0	1	9	0	0	0	Fatal=0, Err
power_guidance	05-20-2014 16:40:59	0:0:28 (28 secs)	Completed	0	0	13	0	0	0	Fatal=0, Err
power_mem_reduction	05-20-2014 16:44:12	0:2:59 (179 secs)	Completed	0	0	13	0	0	0	Fatal=0, Err
selective_autofix@RME_1	05-20-2014 16:45:00	0:0:40 (40 secs)	Completed	0	0	3	0	0	0	Fatal=0, Err
sec@RME_1	05-20-2014 16:45:33	0:0:23 (23 secs)	Completed	0	0	3	0	0	0	Fatal=0, Err
power_est_average@RME_1	N/A		Not started	0	0	0	0	0	0	Fatal=0, Err
power_profiling@RME_1	N/A		Not started	0	0	0	0	0	0	Fatal=0, Err
<b>Summary</b>			<b>Not completed</b>	<b>0</b>	<b>1</b>	<b>50</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>Failed goals</b>

Category	Design Objective	Success Criteria
<b>Power</b>	Internal power = 364.036uW	Not set
	Leakage power = 40.370uW	Not set
	Switching power = 195.229uW	Not set
	Total power = 599.634uW	Not set
<b>Summary</b>		<b>Failed objectives = 0</b>



## SPYGLASS<sup>®</sup> FROM AURELIA DataSheet

RTL Signoff Report

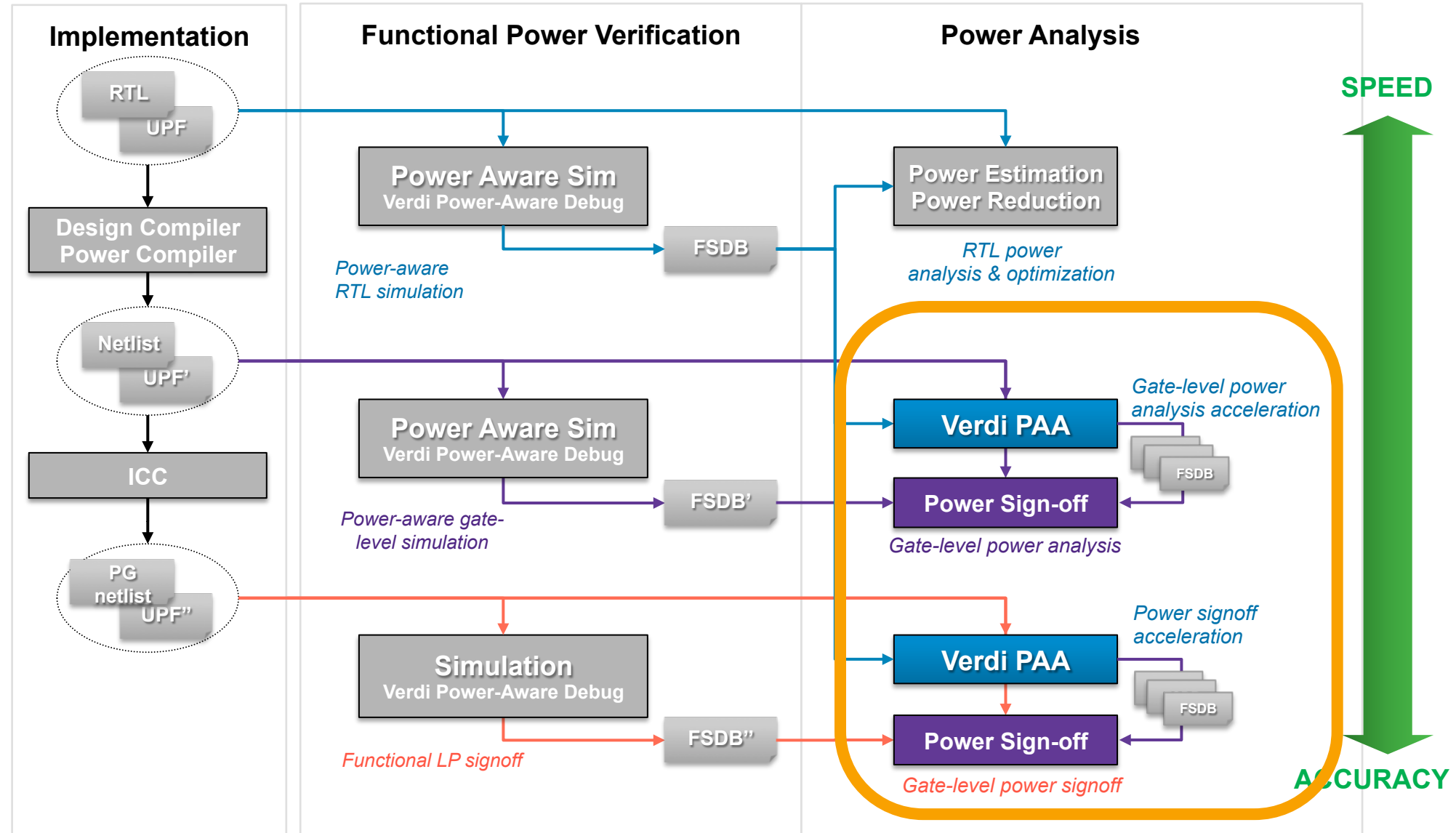
Spyglass Power Estimation/Reduction Report  
Created: Tue May 20 16:45:35 PDT 2014 by guillaume

<b>Power (599.634uW total)</b> <a href="#">Collapse</a>		<b>Power Clocks (3 power clocks)</b> <a href="#">Full Expand</a>	
Technology		Frequency	
dti_sp_tm28hpmhvt_256x32_4ww1x_m_typ_lib, tsmc_130_typical		mr_x_clk_pad_i	
Register bit width threshold for clock gating		12.562MHz	
Registers enabled with clock gating		mt_x_clk_pad_i	
1963 (Total 2346)		33.333MHz	
Number of non gated registers		wb_clk_i	
476		Note: Source of frequency obtained from simulation trace files (VCD,FSDB,SAIF,...etc)	
Clock Gating percentage			
79.719%			
Clock Gating efficiency			
76.54%			
Leakage Power			
40.370uW			
Internal Power			
364.036uW			
Switching Power			
195.229uW			
Total Power			
599.634uW			
Power Savings			
2.061uW			

# Gate Level Power Analysis Acceleration



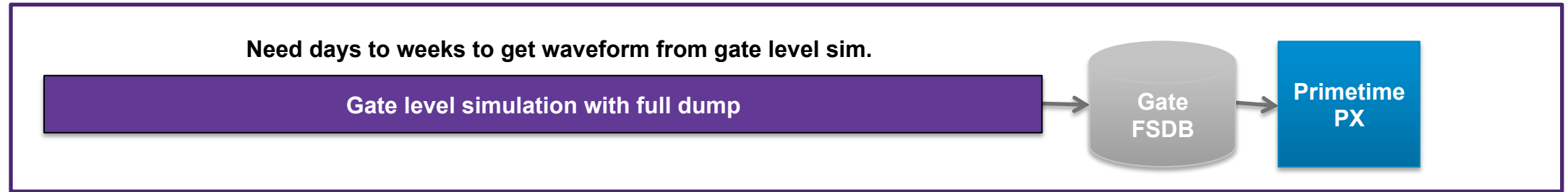
# Synopsys Power Analysis Solutions



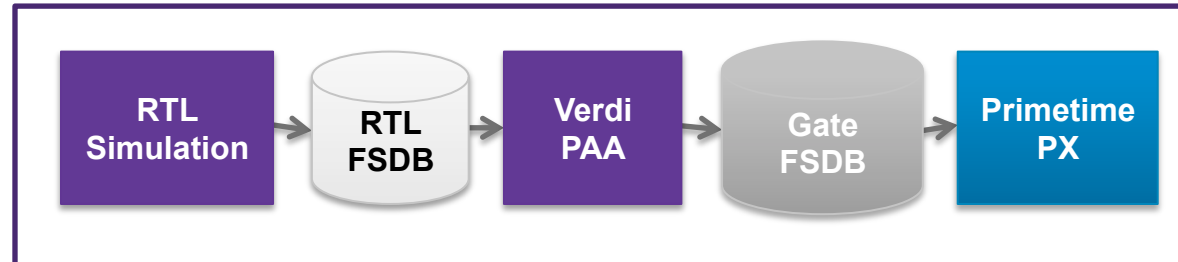
# Power Analysis Acceleration Engine

*Enable Gate Level Power Signoff with RTL Switching Data – Early and faster !!*

Original  
Flow  
(Reference)



Verdi PAA  
Flow



## Verdi Power Analysis Acceleration

- Estimate power before gate level env is ready
- Full range of gate level simulation is not required
- Leverage SDF to improve accuracy

	IDLE mode period		Active mode period	
	Reference	Verdi PAA	Reference	Verdi PAA
Simulation Run time	42 hrs	2 hrs	126 hrs	6 hrs
Time Saving		21X		21X
Total Power (mW)	0.0034	0.0033	0.0729	0.0713
Total Power Tolerance		0%		-2%

21X speedup  
2% difference  
from reference  
flow

# Power Analysis Acceleration

*Uses Siloti Correlation and Siloti Replay Simulation with PrimeTime PX*

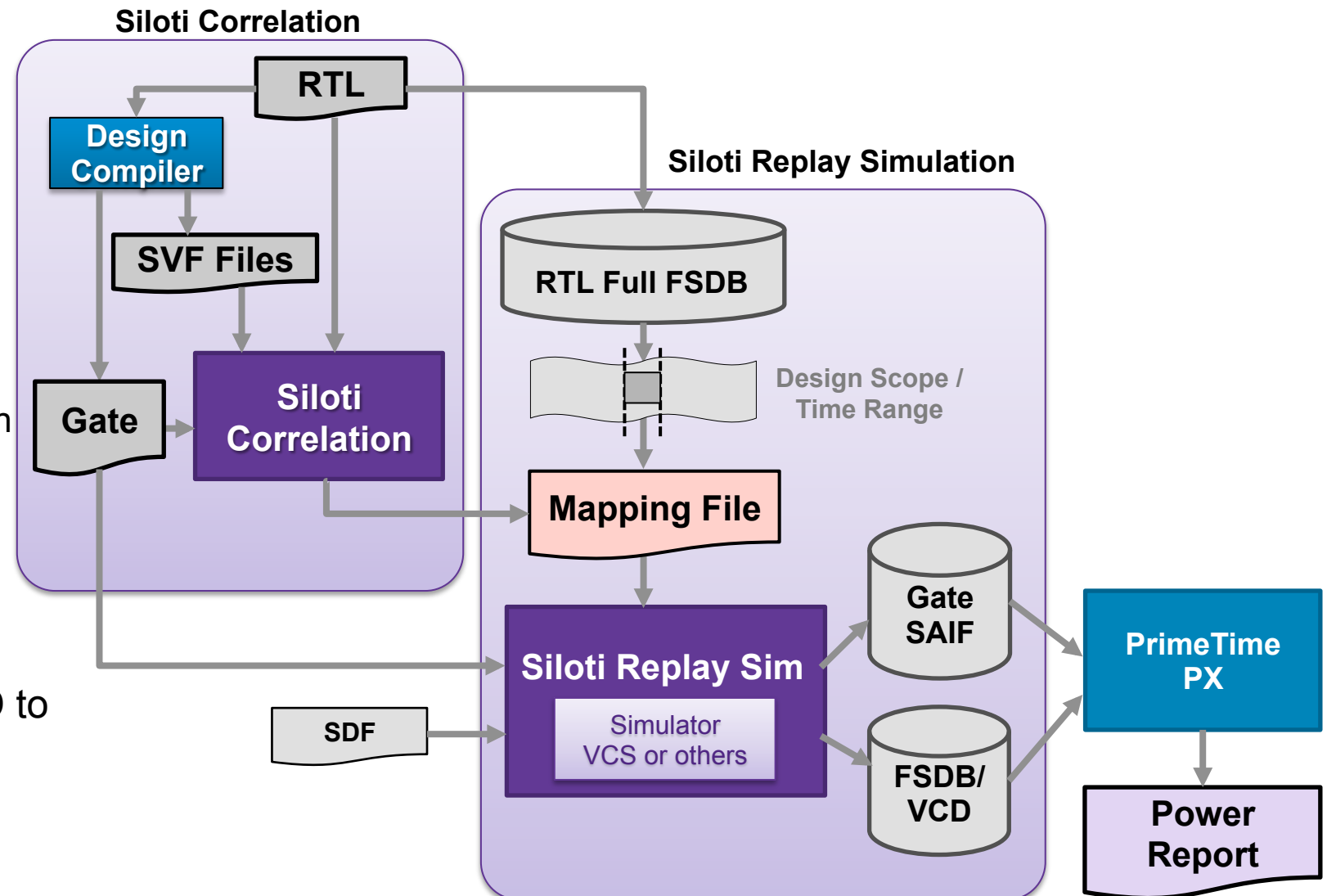
## 1. Siloti Correlation

- Input RTL and netlist designs
- Leverage SVF output from DC
- Generate mapping file

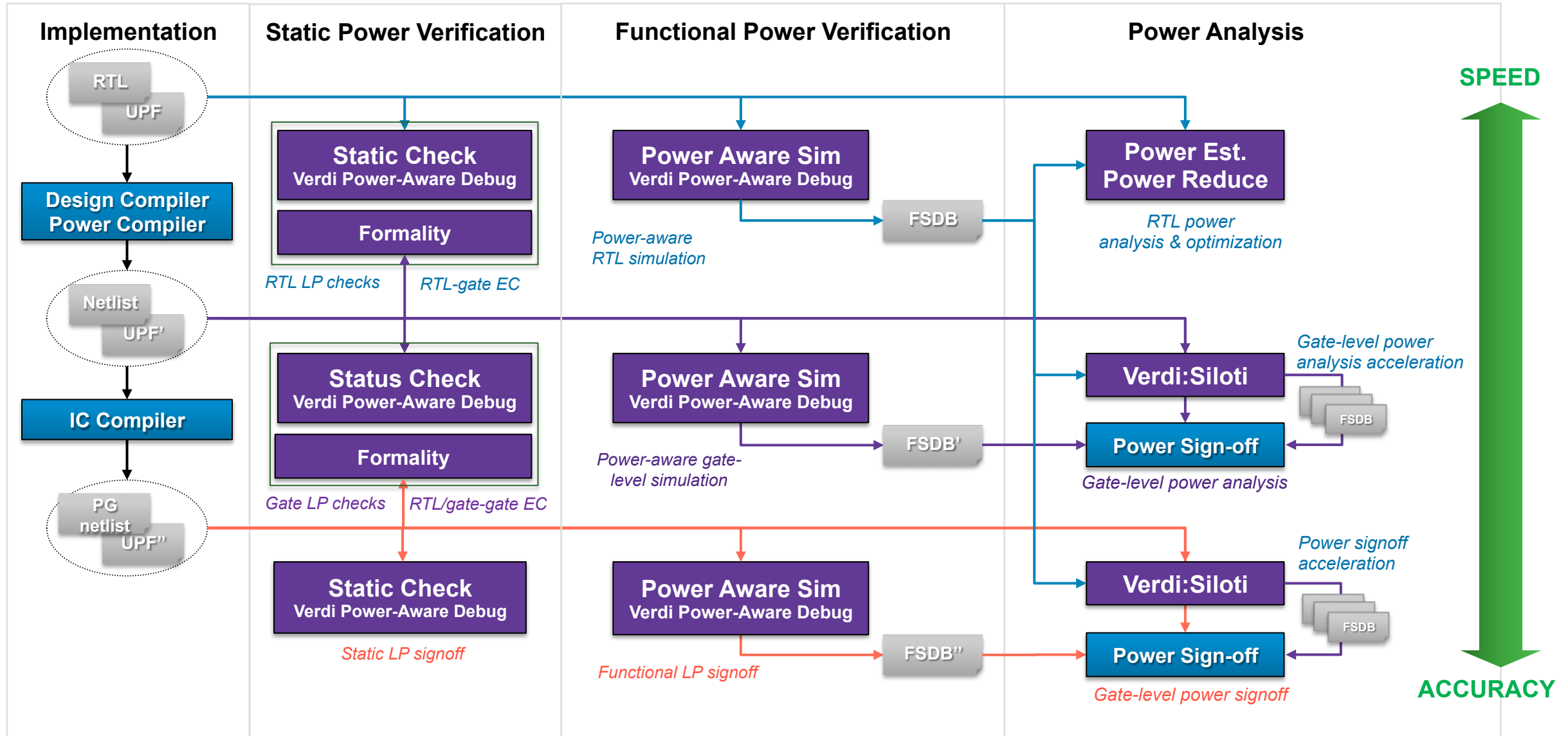
## 2. Siloti Replay Simulation

- Input FSDB from RTL simulation
- Restrict simulation & dumping
- Leverage SDF
- Regenerate gate-level data

## 3. Input gate SAIF or FSDB/VCD to PrimeTime PX



# Synopsys Power Verification & Analysis Solutions



# Q & A

# Thank You

